

## CLAIMS

What is claimed is:

1. A field effect transistor comprising:
  - a substrate having source and drain regions;
  - a gate insulator above said substrate;
  - a notch-shaped gate conductor above said gate insulator, said notch-shaped gate conductor comprising at least two layered sections, including an upper layer and a lower layer,
  - wherein said layered sections comprise at least two different materials, one of which comprises silicon-germanium, and
  - wherein said lower layer has a higher etch rate than said upper layer.
2. The field effect transistor according to claim 1, wherein said upper layer comprises polysilicon-germanium and said lower layer is selected from a group consisting of amorphous silicon and polysilicon.
3. The field effect transistor in claim 2, wherein said amorphous silicon and polysilicon are devoid of germanium.

1        4.        The field effect transistor according to claim 1, wherein said lower layer  
2        and said upper layer comprise polysilicon-germanium (poly-SiGe) having  
3        concentrations of germanium that increase along a depth of said upper layer  
4        section and said lower layer section.

1        5.        The field effect transistor according to claim 4, wherein an increase in said  
2        concentrations of germanium is directly proportional to a depth between a bottom  
3        of said lower layer and a top of said upper layer.

1        6.        The field effect transistor in claim 1, wherein said upper layer and said  
2        lower layer comprise materials capable of being simultaneously etched.

1        7.        A field effect transistor comprising:  
2        a substrate having source and drain regions;  
3        a gate insulator above said substrate;  
4        a notch-shaped gate conductor above said gate insulator, said notch-shaped  
5        gate conductor comprising at least two layered sections, including an upper layer  
6        and a lower layer,  
7        wherein said upper layer comprises polysilicon and said lower layer  
8        comprises amorphous silicon, and  
9        wherein said lower layer has a higher etch rate than said upper layer.

1 8. The field effect transistor according to claim 7, wherein said upper layer  
2 section comprises polysilicon-germanium.

1 9. The field effect transistor in claim 8, wherein said amorphous silicon is  
2 devoid of germanium.

1 10. The field effect transistor in claim 7, wherein said upper layer and said  
2 lower layer comprise materials capable of being simultaneously etched.

1 11. A method for making a field effect transistor having a notch-shaped gate  
2 conductor, said method comprising:

3 forming a gate insulator above a substrate;

4 depositing a gate conductor material over said gate insulator, wherein said  
5 gate conductor material comprises at least two layered sections, including an  
6 upper layer and a lower layer, said layered sections comprising at least two  
7 different materials, one of which comprises silicon-germanium, and said lower  
8 layer having a higher etch rate than said upper layer;

9 etching said gate conductor material through a mask to define a notch-  
10 shaped gate conductor;

11           doping said notch-shaped gate conductor and said substrate, to make said  
12 notch-shaped gate conductor conductive, and to form source and drain regions in  
13 said substrate.

1       12.    The method in claim 11, wherein said upper layer comprises polysilicon-  
2 germanium and said lower layer is selected from a group consisting of amorphous  
3 silicon and polysilicon.

1       13.    The method in claim 12, wherein said amorphous silicon and polysilicon  
2 are devoid of germanium.

1       14.    The method in claim 11, wherein said lower layer and said upper layer  
2 comprise polysilicon-germanium (poly-SiGe) having concentrations of  
3 germanium that increase along a depth of said upper layer section and said lower  
4 layer section.

1       15.    The method in claim 14, wherein an increase in said concentrations of  
2 germanium is directly proportional to a depth between a bottom of said lower  
3 layer and a top of said upper layer.

1 16. The method in claim 11, wherein said etching of said gate conductor  
2 material comprises a single etching process.

1 17. A method for making a field effect transistor having a notch-shaped gate  
2 conductor, said method comprising:  
3 forming a gate insulator above a substrate;  
4 depositing a gate conductor material over said gate insulator, wherein said  
5 gate conductor material comprises at least two layered sections, including an  
6 upper layer and a lower layer, said upper layer comprising polysilicon, said lower  
7 layer comprising amorphous silicon, and said lower layer having a higher etch rate  
8 than said upper layer;  
9 etching said gate conductor material through a mask to define a notch-  
10 shaped gate conductor; and  
11 doping said notch-shaped gate conductor and said substrate, to make said  
12 notch-shaped gate conductor conductive, and to form source and drain regions in  
13 said substrate.

1 18. The method in claim 17, wherein said upper layer section comprises  
2 polysilicon-germanium.

1 19. The method in claim 18, wherein said amorphous silicon is devoid of  
2 germanium.

1 20. The method in claim 17, wherein said etching of said gate conductor  
2 material comprises a single etching process.

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